IT IS CLAIMED:

1. In a non-volatile memory having an array of memory storage units, each unit having a charge storage unit between a control gate and a channel region defined by a source and a drain, and a bit line switchably coupled to the drain, a method of programming in parallel a page of memory storage units having a common word line interconnecting their control gates, comprising:

(a) providing a bit line for each memory storage unit of the page, switchably coupled to the drain thereof;

(b) determining for each of those memory storage units of the page slated to be programmed whether or not its neighboring memory storage units are in a program inhibit mode;

(c) for those memory storage units of the page slated to be program inhibited, applying a first predetermined voltage to each of the bit lines thereof to inhibit programming;

(d) applying a second predetermined voltage to each bit line of those memory storage unit of the page slated to be programmed to enable programming, said second predetermined voltage for said each bit line being a function of the operation mode of its neighboring memory storage units so as to offset any perturbation therefrom; and

(e) applying a programming voltage pulse to said word line in order to program in parallel the memory storage units of the page, wherein those memory storage units having a bit line with said first predetermined voltage are program-inhibited by virtue of their floated channel boosted to a program inhibited voltage condition, and a perturbation resulted from the boosting on any neighboring programming memory storage unit is compensated by said offsetting from said second predetermined voltage.

2. The method as in claim 1, further comprising:

(f) verifying if any of the memory storage units under programming has been programmed to its target state;

(g) designating any memory storage units that have been verified to be slated for program inhibition and any memory storage units that have not been verified to be for programming; and

(h) repeating (c) to (g) until all of said page of memory storage units have been verified.

3. The method as in any one of claims 1 or 2, wherein the operation mode of at least one of the neighboring memory storage units is derivable from a sense module coupled thereto.

4. The method as in any one of claims 1 or 2, wherein the operation mode of at least one of the neighboring memory storage units is derivable from a voltage of the bit line coupled thereto.

5. The method as in any one of claims 1 or 2, wherein said page of memory storage units forms a contiguous row of said array.

6. The method as in any one of claims 1 or 2, wherein said page of memory storage units forms a contiguous segment of a row of said array.

7. The method as in any one of claims 1 or 2, wherein:

said memory is organized as an array of NAND chains of memory storage units, each chain having a plurality of memory storage units connected in series, and said page of memory storage units is constituted from a memory storage unit from each NAND chain among a page thereof.

8. The method as in any one of claims 1 or 2, wherein each memory storage unit stores one bit of information.

9. The method as in any one of claims 1 or 2, wherein each memory storage unit stores more than one bit of information.

10. The method as in any one of claims 1 or 2, wherein said charge storage unit is a floating gate.

11. The method as in any one of claims 1 or 2, wherein said charge storage unit is a dielectric layer.

12. The method as in any one of claims 1 or 2, wherein said non-volatile memory is in the form of a memory card.

13. A non-volatile memory comprising:

an array of memory storage unit arranged in rows and columns;

each memory storage unit having a charge storage unit, a control gate and a channel region defined by a source and a drain;

a word line interconnecting the control gates of a page of memory storage units;

a bit line for each memory storage unit of said page, said bit line switchably coupled to the drain thereof;

a precharging circuit coupled to said bit line,

said precharging circuit supplying a predetermined program inhibiting voltage to said bit line when the associated memory storage unit is slated for program inhibition and

supplying a predetermined program enabling voltage said bit line when the associated memory storage unit is slated for programming, and

said predetermined program enabling voltage having a predetermined offset that is a function of whether or not none, one, or both of neighboring memory storage units are in a program inhibit mode.

14. A non-volatile memory as in claim 13, further comprising:

individual sense modules associated with said neighboring memory storage units and wherein a signal from each said individual sense module indicates whether the associated neighboring memory storage is in a program inhibit mode or not.

15. A non-volatile memory as in claim 13, further comprising:

individual bit line voltage detectors associated with said neighboring memory storage units and wherein a signal from each said individual bit line voltage detector indicates whether the associated neighboring memory storage is in a program inhibit mode or not.

16. A non-volatile memory, comprising:

an array of memory storage units, each unit having a charge storage unit between a control gate and a channel region defined by a source and a drain;

a word line interconnecting the control gates of a page of memory storage units of said array;

a bit line for each memory storage unit of the page, switchably coupled to the drain thereof;

means for applying a first predetermined voltage to inhibit programming to each of the bit lines of those memory storage units of the page slated to be program inhibited;

means for determining for each of those memory storage units of the page slated to be programmed whether or not its neighboring memory storage units are in a program inhibit mode;

means for applying a second predetermined voltage to each bit line of those memory storage unit of the page slated to be programmed to enable programming, said second predetermined voltage for said each bit line being a function of the operation mode of its neighboring memory storage units so as to offset any perturbation therefrom; and

means for applying a programming voltage pulse to said word line in order to program in parallel the memory storage units of the page, wherein those memory storage units having a bit line with said first predetermined voltage are program-inhibited by virtue of their floated channel boosted to a program inhibited voltage condition, and a perturbation resulted from the boosting on any neighboring programming memory storage unit is compensated by said offsetting from said second predetermined voltage.

17. The non-volatile memory as anyone of claims 13-15, wherein said page of memory storage units forms a row of said array.

18. The non-volatile memory as in anyone of claims 13-15, wherein said page of memory storage units forms a segment of a row of said array.

19. The non-volatile memory as in anyone of claims 13-15, wherein:

said memory is organized as an array of NAND chains of memory storage units, each chain having a plurality of memory storage units connected in series, and said page of memory storage units is constituted from a memory storage unit from each NAND chain among a page thereof.

20. The non-volatile memory as in anyone of claims 13-15, wherein each memory storage unit stores one bit of information.

21. The non-volatile memory as in anyone of claims 13-15, wherein each memory storage unit stores more than one bit of information.

22. The non-volatile memory as in anyone of claims 13-15, wherein said charge storage unit is a floating gate.

23. The non-volatile memory as in anyone of claims 13-15, wherein said charge storage unit is a dielectric layer.

24. The non-volatile memory as in anyone of claims 13-15, wherein said non-volatile memory is in the form of a card.

25. A non-volatile memory, comprising:

an array of memory storage units;

a group of memory storage units among said array, each memory storage unit of the group having a bit line coupled thereto;

a circuit for operating on said group of memory storage units in parallel while individual memory storage units of the group exist in one of a predetermined set of operation modes; and

said circuit further comprising a voltage supply for supplying selected one of a predetermined set of voltages to each bit line; said selected voltage being a function of the operation modes of neighboring memory storage units.